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REMARKS

Claims 1-27 are pending herein. In the Office Action, claims 1-3 were rejected under 35 U.S.C. §102(b) as being anticipated by US Pat. No. 6,127,862 to Kawasumi (hereinafter "Kawasumi"), and claims 1-9, 11-14, 18-22 and 24-27 were rejected under 35 U.S.C. §102(b) as being anticipated by US Pat. No. 5,457,407 to Shu et al. (hereinafter "Shu").

Claims 10, 15-17 and 23 were objected to as being dependent upon a rejected base claim, but were otherwise considered allowable.

Preliminarily, the Specification is amended to replace paragraph [0002] in its entirety in which the missing serial number information is provided. Applicant respectfully requests approval of this amendment.

Applicant respectfully traverses the §102(b) rejection of claims 2-3 as being anticipated by Kawasumi.

Kawasumi does not show or suggest a binary array of matched impedance devices as recited in claims 2 and 3. As shown in FIG. 3 and as described in paragraphs [0039] – [0040] of the present application as filed, a binary array of devices means that the devices are binarily grouped (page 19, lines 3-8). As shown in FIG. 3, the devices are grouped in binary progression based on 2^N for $N = 0, 1, 2, \dots$, etc., (e.g., 1, 2, 4, 8, 16, etc.). In particular, the first "group" includes 1 device N1, the second group 301 includes 2 devices N3:N2, the third group 303 includes 4 devices N7:N4, the fifth group 305 includes 8 devices N15:N8, the sixth group 307 includes 16 devices N31:N16, and the

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seventh group 309 includes 32 devices N63:N32. Kawasumi says very little about the relative values of the impedances within any given array other than that they are "different from each other" (col. 7, lines 6-8). Applicant respectfully submits, therefore, that claims 2 and 3 are allowable over Kawasumi and requests withdrawal of this rejection.

Applicant respectfully traverses the §102(b) rejection of claims 2-3, 7-9, 18, 25 and 27 as being anticipated by Shu.

Shu does not show or teach bias adjustment logic as recited in claims 7 and 8. Contrary to that stated in the Office Action, the comparator 6 in FIG. 2 of Shu does not comprise bias adjustment logic that combines a bias amount with a reference impedance control input as recited in claim 7. The comparator 6 produces an up/down signal to adjust the impedance across terminals A and B of the "lower transistor array" until the potentials of the VMID and VLHALF nodes match (Shu, col. 1, lines 50-58). And, when the potentials of the VMID and VLHALF nodes match, then the impedances of the "lower transistor array" and the reference resistor R1 match each other. Yet Shu does not show bias adjustment beyond the match point to provide further adjustment as recited in claim 7. Applicant respectfully submits, therefore, that claim 7 is allowable over Shu. Claim 8 is allowable as depending upon allowable claim 7. Furthermore, the comparator 6 of Shu is not described as being "programmable" as recited in claim 8. Applicant requests withdrawal of these rejections of claims 7 and 8.

In a similar manner, Shu does not show or teach programming a bias adjust value and combining the bias adjust value with a reference impedance input as recited in claim

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25. There is no discussion or teaching or circuitry addressing bias adjust values at all including combining such a value to reference inputs. Applicant requests withdrawal of the rejection of claim 25.

Shu does not show or teach an impedance matching controller comprising first and second controllers as recited in claim 9.

It is first noted that the "line connected to external R4 to circuit" does not form a first controller and that the "line connected to R3 to connected (sic) to circuit" does not form a second controller. Claim language should be given its ordinary and customary meaning and interpreting a connection line as a controller is not ordinary or customary and thus is improper.

Furthermore, claim 1 recites an impedance matching controller which adjusts the reference impedance control input until a *reference impedance* matches a *reference value*. In claim 9, which depends on claim 1, the impedance matching controller comprises a first controller for coupling to an external reference resistor that provides the first reference value and a second controller including an internal reference resistor that provides a second reference value. In Shu, the resistor R2 is used as part of a voltage divider which divides VDD by a ratio to provide the VMID voltage. Thus, the resistor R2 in Shu is not a reference value for adjusting the reference impedance, since the actual resistance of R2 is arbitrary and depends upon the input impedance of the LPF 2 and/or comparator 6 (Shu, FIG. 2). In Shu's illustrated embodiment, as long as the ratio of the resistances of R2 and R3 are suitable to set the desired voltage level of VMID, their nominal values are irrelevant, at least for purposes of adjusting the reference impedance.

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Applicant respectfully submits, therefore, that claim 9 is allowable over Shu and requests withdrawal of this rejection.

Shu does not show a binary array of matched impedance devices as recited in claims 2, 3, 18 and 27. As discussed above, a binary array of devices means that the devices, which are matched with each other, are binarily grouped. In Shu, the reference transistors are not matched but instead have varying widths which vary based on a binary fraction relative to each other (See Abstract of Shu). Applicant respectfully submits, therefore, that claims 2, 3, 18 and 27 are allowable over Shu and requests withdrawal of this rejection.

Claim 1 is amended to recite an output driver impedance controller with an internal reference value and an external reference value and an impedance matching controller which adjusts a reference impedance control input to match a reference impedance with a selected one of said first and second reference values. Applicant respectfully submits that neither Kawami nor Shu show or teach an output driver impedance controller using a selected one of an internal reference value and an external reference value as recited in claim 1. Both Kawasumi and Shu assume a single reference element which is provided externally or outside the main circuit. In Kawasumi, the "dummy resistance element Rd" (Kawasumi, col. 6, line 16) is the only reference element and it is typically provided "outside" (Kawasumi, col. 10, lines 50-62). In Shu, the only reference element is externally-coupled R1 (Shu, col. 1, lines 62-63) for the circuit of FIG. 2 or "external reference resistor" R4 of the circuit of FIG. 3.

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At least one advantage of more than one reference resistor is that one may be used as a default in the event the other is not provided, disconnected, or damaged. In an integrated circuit embodiment for example, an internal default reference resistor is employed in the event an external reference resistor is unavailable for any reason so that the circuit may operate without it.

Applicant respectfully submits that amended claim 1 is allowable over Kawasumi and is further allowable over Shu. Claims 2-9 and 11 are allowable as depending upon allowable claim 1. Claims 5 and 9 are amended to conform with amended claim 1.

Claim 12 is amended to recite an IC including impedance matching logic, which further includes an external reference resistor, an internal reference resistor, and comparator logic that adjusts a reference impedance control input to equalize values of a selected one of the internal and external reference resistors. In a similar manner as described above, Applicant respectfully submits that neither Kawami nor Shu show or teach an IC with comparator logic that adjusts a reference impedance control input to equalize values of selected one of an internal reference value and an external reference value as recited in claim 12. Applicant respectfully submits that amended claim 12 is allowable over Kawasumi and is further allowable over Shu. Claims 13-14 and 18-20 are allowable as depending upon allowable claim 1. Claims 13, 14 and 19 are amended to conform with amended claim 12.

Claim 21 is amended to recite method of controlling pull-down impedance of at least one output driver including providing an internal reference resistor for use when an external reference resistor is unavailable and selecting between the internal and external

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reference resistors. In a similar manner as described above, Applicant respectfully submits that neither Kawami nor Shu show or teach a method of controlling pull-down impedance including selecting between the internal and external reference resistors as recited in claim 21. Applicant respectfully submits that amended claim 21 is allowable over Kawasumi and is further allowable over Shu. Claims 22 and 24-25 are allowable as depending upon allowable claim 21. Claims 22 and 23 are amended to conform with amended claim 21.

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CONCLUSION

Applicant respectfully submits that for the reasons recited above and for various other reasons, the objections and rejections have been overcome and should be withdrawn. Applicant respectfully submits therefore that the present application is in a condition for allowance and reconsideration is respectfully requested. Should this response be considered inadequate or non-responsive for any reason, or should the Examiner have any questions, comments or suggestions that would expedite the prosecution of the present case to allowance, Applicants' undersigned representative earnestly requests a telephone conference.

Respectfully submitted,

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By: /Gary Stanford/
Gary R. Stanford Reg. No. 35,689

Customer Number 23669